REMARKS

This responds to the Advisory Action mailed December 8, 2006 and the Final Office Action mailed on September 14, 2006.

Claims 2-6, 9-11, 16, 29 and 31 are amended, claims 1, 7-8, 12-15, 28, 30 and 32 are canceled, and claims 34-49 are added; as a result, claims 2-6, 9-11, 16-27, 29, 31, and 33-49 are pending in this application.

The Advisory Action of December 8, 2006 indicated that the "Newly proposed claim(s) or amended claim(s) 17-27, 29, 31, 33 would be allowable if submitted in a separate, timely filed canceling the non-allowable claims(s)." These corresponding claims in their allowable form are included in this amendment and response.

Claim 1 has been canceled. The dependencies of claims 2-6 and 9-11, which previously depended from claim 1, have been amended to depend from allowable claim 17. It thus submitted that claims 2-6 and 9-11 are also allowable. Claims 7-8 and 12-15 have been canceled.

Claim 12 has also been canceled. The dependency of claim 16, which previously depended from claim 12, has been amended to depend from allowable claim 23. It thus submitted that claim 16 is also allowable. Claims 12-15 have been canceled.

New claim 34 corresponds to allowed claim 17. It is submitted that claim 34 is also allowable. Basis for the new claim can be found in several places throughout the filed application as shown by way of example below. Dependent claims 35-42 correspond to dependent claims 2-6 and 9-11, respectively. As claim 34 is allowable, claims 2-6 and 9-11 are also allowable.

New claim 43 corresponds to allowed claim 23. It is submitted that claim 43 is also allowable. Basis for the new claim can be found in several places throughout the filed application as shown by way of example below. Dependent claims 43-47 correspond to dependent claims 24-27, respectively. As claim 43 is allowable, claims 43-47 are also allowable.

New claims 48 and 49 correspond to canceled claims 28 and 31, respectively. As claims 48 and 49 are dependent upon claims 17 and 23 they are also allowable.

Basis in the written description for the modified claims 34 and 43 (e.g., in programmable or fixed form) and their dependent claims can be found in several places throughout the drawings and written description, examples of which are provided below:

Fig. 5 is a *block diagram* of a signal processing system suitable for implementing the present invention.

Interconnect block 518, which in one embodiment is an **application-specific integrated circuit (ASIC)**, serves to interconnect and buffer between the various operational units.
(Page 12, paragraph 3)

It is also possible to design interconnect block 518 to perform the functions of DSP 520 in either a programmable or fixed algorithm form. Similarly, the DSP program can be contained in interconnect block 518, as can temporary information storage, if interconnect block 518 is an ASIC.
(Page 12, last paragraph)

Fig. 6 is a *block diagram* of a sample rate converter, in accordance with the present invention.

This is achieved by having an upsampling filter 602 coupled to an interpolator 604 such that the data sample x_n are received by the filter 602.
(Page 13, paragraph 1)

Fig. 9 is a simplified plan view of a *compensating circuit* where a first order allpass filter partially compensates phase nonlinearity of a power symmetric elliptical half-band filter, in accordance with the present invention.

Fig. 11 is a *block diagram* of a sample rate converter, in accordance with an alternate embodiment of the present invention.

To that end, the converter 1100 includes a half-band filter 1102 coupled to an interpolator 1104 such that the data samples x^1_n are received by the filter 1102. Such a configuration is particularly useful for converting from a sample rate of nominally 96 kHz to a local 48 kHz rate.
(Page 19, lines paragraph 2).

Fig. 13 is a *block diagram* of a sample rate converter, in accordance with a second alternate embodiment of the present invention.

Referring to Figs. 5 and 13, were the output sample rate less than or approximately equal to the input sample rate, but well above half of the same, then it would be preferred to have a sample rate converter 1300 with an interpolator 1304 producing an intermediate signal at exactly twice the output sample rate. The interpolator 1304 is followed by a half-band decimating filter 1306 having a sharp cutoff.

Fig. 15 is a block diagram of a sample rate converter, in accordance with a second alternate embodiment of the present invention.

Referring to Fig. 15, the advantage of the preferred embodiment of the interpolator in all of the aforementioned sample rate converters is that it facilitates providing a dynamically changing sample rate. As a result, the sample rate ratio may dynamically change. Consider, for example, a sample rate converter 1500 that provides sample rate ratios from slightly more than 1/3 to infinity (in practice an arbitrarily high value). In this case, the input signal x^2_n is first upsampled by a factor of two using a half-band upsampling filter 1502. The sample rate is then converted to twice the desired output rate using a wide transition band interpolator 1504. Finally, the output of the interpolator is decimated by a factor of two using a half-band decimating filter 1506, as described above producing output signal y^2_m.
(Page 22, paragraph 3)

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney 408-278-4041 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 14th, day of February 2007.

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